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L5	609	analog digital parallel order change	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2005/06/24 07:36
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L7	363	analog digital parallel order	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/06/24 07:37
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IEE CNF	IEE Conference Proceeding
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1. **Algorithmic partial analog-to-digital conversion in mixed-signal array processors**
Genov, R.; Cauwenberghs, G.;
Circuits and Systems, 2003. ISCAS '03. Proceedings of the 2003 International Sympos
Volume 1, 25-28 May 2003 Page(s):I-769 - I-772 vol.1
AbstractPlus | Full Text: PDF(339 KB) IEEE CNF

2. **Charge-mode parallel architecture for vector-matrix multiplication**
Genov, R.; Cauwenberghs, G.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [s
and Systems II: Express Briefs, IEEE Transactions on]
Volume 48, Issue 10, Oct. 2001 Page(s):930 - 936
AbstractPlus | References | Full Text: PDF(205 KB) IEEE JNL

3. **Highly parallel pulsed optoelectronic analog-digital converter**
Kang, J.U.; Frankel, M.Y.; Esman, R.D.;
Photonics Technology Letters, IEEE
Volume 10, Issue 11, Nov. 1998 Page(s):1626 - 1628
AbstractPlus | References | Full Text: PDF(56 KB) IEEE JNL

4. **A parallel switch-level simulator for mixed analog-digital circuit simulation**
Molin, B.-A.; Mattisson, S.;
Design Automation, 1992. Proceedings. [3rd] European Conference on
16-19 March 1992 Page(s):202 - 206
AbstractPlus | Full Text: PDF(300 KB) IEEE CNF

5. **Proceedings of 36th Midwest Symposium on Circuits and Systems**
Circuits and Systems, 1993., Proceedings of the 36th Midwest Symposium on
16-18 Aug. 1993
AbstractPlus | Full Text: PDF(104 KB) IEEE CNF

6. **Error analysis of parallel analogue to digital converters**
Fernandes, J.R.; Silva, M.M.;
Circuits and Systems, 1994. ISCAS '94., 1994 IEEE International Symposium on
Volume 5, 30 May-2 June 1994 Page(s):341 - 344 vol.5
AbstractPlus | Full Text: PDF(300 KB) IEEE CNF

7. **Charge-mode parallel architecture for matrix-vector multiplication**
Genov, R.; Cauwenberghs, G.;
Circuits and Systems, 2000. Proceedings of the 43rd IEEE Midwest Symposium on
Volume 1, 8-11 Aug. 2000 Page(s):506 - 509 vol.1
AbstractPlus | Full Text: PDF(376 KB) IEEE CNF

8. **Parallel, high-speed PC fuzzy control**
Jaramillo-Botero, A.; Miyake, Y.;
Micro, IEEE
Volume 15, Issue 6, Dec. 1995 Page(s):63
AbstractPlus | Full Text: PDF(88 KB) IEEE JNL

9. **Gigahertz waveform sampling and digitization circuit design and implementation**
Kleinfelder, S.;
Nuclear Science, IEEE Transactions on
Volume 50, Issue 4, Aug. 2003 Page(s):955 - 962
AbstractPlus | References | Full Text: PDF(827 KB) IEEE JNL

10. **A parallel routing technique based on local current comparison**
Cheng, G.-X.; Tanaka, M.; Yamada, M.;
Circuits and Systems, 1991., IEEE International Sympoisum on
11-14 June 1991 Page(s):3114 - 3117 vol.5
AbstractPlus | Full Text: PDF(280 KB) IEEE CNF

11. **VLSI Hamming neural net showing digital decoding**
Gomez-Castaneda, F.; Moreno-Cadenas, J.A.;
Neural Networks for Signal Processing [1993] III. Proceedings of the 1993 IEEE-SP W
6-9 Sept. 1993 Page(s):405 - 410
AbstractPlus | Full Text: PDF(196 KB) IEEE CNF

12. **High speed VLSI neural network for high-energy physics**
Masa, P.; Hoen, K.; Wallinga, H.;
Microelectronics for Neural Networks and Fuzzy Systems, 1994., Proceedings of the F
Conference on
26-28 Sept. 1994 Page(s):422 - 428
AbstractPlus | Full Text: PDF(584 KB) IEEE CNF

13. **VLSI neural network implementation of a hippocampal model**
Sheu, B.J.; Berger, T.W.; Wu, T.H.; Tsai, R.H.;
Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on
Volume 3, 28 April-3 May 1995 Page(s):1664 - 1667 vol.3
AbstractPlus | Full Text: PDF(356 KB) IEEE CNF

14. **A multi-GHz, multi-channel transient waveform digitization integrated circuit**
Kleinfelder, S.;
Nuclear Science Symposium Conference Record, 2002 IEEE
Volume 1, 10-16 Nov. 2002 Page(s):544 - 548 vol.1
AbstractPlus | Full Text: PDF(2609 KB) IEEE CNF

15. **A fully digital real-time simulator for protective relay testing**
Kuffel, R.; Giesbrecht, J.; Maguire, T.; Wierckx, R.P.; Forsyth, P.A.; McLaren, P.G.;
Developments in Power System Protection, Sixth International Conference on (Conf. P
25-27 March 1997 Page(s):147 - 150
AbstractPlus | Full Text: PDF(476 KB) IEE CNF

16. **Error diffusion coding for A/D conversion**
Anastassiou, D.;

Circuits and Systems, IEEE Transactions on
Volume 36, Issue 9, Sept. 1989 Page(s):1175 - 1186

AbstractPlus | Full Text: PDF(1188 KB) IEEE JNL

☐ **17. Micromechanical digital-to-analog converter for out-of-plane motion**
Guangya Zhou; VJ, Logeeswaran.; Tay, F.E.H.; Fook Siong Chau;
Microelectromechanical Systems, Journal of
Volume 13, Issue 5, Oct. 2004 Page(s):770 - 778

AbstractPlus | References | Full Text: PDF(1864 KB) IEEE JNL

☐ **18. Parallel-path digital-to-analog converters for Nyquist signal generation**
Deveugele, J.; Palmers, P.; Steyaert, M.S.J.;
Solid-State Circuits, IEEE Journal of
Volume 39, Issue 7, July 2004 Page(s):1073 - 1082

AbstractPlus | References | Full Text: PDF(632 KB) IEEE JNL

☐ **19. A low-cost PC-based virtual oscilloscope**
Bhunia, C.; Giri, S.; Kar, S.; Haldar, S.; Purkait, P.;
Education, IEEE Transactions on
Volume 47, Issue 2, May 2004 Page(s):295 - 299

AbstractPlus | Full Text: PDF(264 KB) IEEE JNL

☐ **20. A multichannel pipeline analog-to-digital converter for an integrated 3-D ultrasou system**
Kaviani, K.; Oralkan, O.; Khuri-Yakub, P.; Wooley, B.A.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 7, July 2003 Page(s):1266 - 1270

AbstractPlus | References | Full Text: PDF(408 KB) IEEE JNL

☐ **21. Calibration of parallel /spl Delta//spl Sigma/ ADCs**
Batten, R.D.; Eshraghi, A.; Fiez, T.S.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [s and Systems II: Express Briefs, IEEE Transactions on]
Volume 49, Issue 6, June 2002 Page(s):390 - 399

AbstractPlus | References | Full Text: PDF(341 KB) IEEE JNL

☐ **22. Effects of crosstalk in demultiplexers for photonic analog-to-digital converters**
Williamson, R.C.; Juodawlkis, P.W.; Wasserman, J.L.; Betts, G.E.; Twichell, J.C.;
Lightwave Technology, Journal of
Volume 19, Issue 2, Feb. 2001 Page(s):230 - 236

AbstractPlus | References | Full Text: PDF(132 KB) IEEE JNL

☐ **23. Cascaded parallel oversampling sigma-delta modulators**
Xuesheng Wang; Wei Qin; Xieting Ling;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [s and Systems II: Express Briefs, IEEE Transactions on]
Volume 47, Issue 2, Feb. 2000 Page(s):156 - 161

AbstractPlus | References | Full Text: PDF(152 KB) IEEE JNL

☐ **24. Smart CMOS focal plane arrays: a Si CMOS detector array and sigma-delta analo converter imaging system**
Joo, Y.; Park, J.; Thomas, M.; Chung, K.S.; Brooke, M.A.; Jokerst, N.M.; Wills, D.S.;
Selected Topics in Quantum Electronics, IEEE Journal of
Volume 5, Issue 2, March-April 1999 Page(s):296 - 305

AbstractPlus | References | Full Text: PDF(1296 KB) IEEE JNL

☐ **25. High-Speed Digital and Analog Parallel Transmission Technique Over Single Tel**

Akashi, F.; Sato, Y.; Eguchi, M.;
Communications, IEEE Transactions on [legacy, pre - 1988]
Volume 30, Issue 5, May 1982 Page(s):1213 - 1218
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1 Sensors: the next wave of innovation

Paul Saffo

February 1997 **Communications of the ACM**, Volume 40 Issue 2

Full text available: pdf(192.99 KB) Additional Information: full citation, citings, index terms

2 Mixed analog-digital design: Digital background and blind calibration for clock skew error in time-interleaved analog-to-digital converters

David Camarero, Jean-François Naviner, Patrick Loumeau

September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(146.26 KB) Additional Information: full citation, abstract, references, index terms

This paper deals with the problem of clock skew errors in time-interleaved analog-to-digital converters. Deterministic sample-time errors between time-interleaved channels generate nonlinear distortion and degrade SFDR. We propose a fully digital calibration method that uses, on the one hand, adaptive FIR filters to reconstruct a correctly sampled signal and, on the other hand, a new blind clock skew detection algorithm that guides the adaptive filters. This calibration method applies to any num ...

Keywords: adaptive filters, clock skew, digital calibration, parallel ADC, sample-time errors, time-interleaved

3 Closing the gap between analog and digital

Khaled Saab, Naim Ben Hamida, Bozena Kaminska

June 2000 **Proceedings of the 37th conference on Design automation**

Full text available: pdf(94.67 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a highly effective method for parallel hard fault simulation and test specification development. The proposed method formulates the fault simulation problem as a problem of estimating the fault value based on the distance between the output parameter distribution of the fault-free and the faulty circuit. We demonstrate the effectiveness and practicality of our proposed method by showing results on different designs. This approach extended by parametric fault test ...

Keywords: fault modeling, fault simulation, hard faults, test vector generation

4 A hardware/software co-design flow and IP library based on simulink
L. M. Reyneri, F. Cucinotta, A. Serra, L. Lavagno
June 2001 **Proceedings of the 38th conference on Design automation**

Full text available: pdf(119.94 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a design flow for data-dominated embedded systems. We use The Mathworks' Simulink\trademark environment for functional specification and algorithmic analysis. We developed a library of Simulink blocks, each parameterized by design choices such as implementation (software, analog or digital hardware, \ldots) and numerical accuracy (resolution, S/N ratio). Each block is equipped with empirical models for cost (code size, chip area) and performance (timing, energy), based ...

5 Power optimization using divide-and-conquer techniques for minimization of the number of operations
Inki Hong, Miodrag Potkonjak, Ramesh Karri
October 1999 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 4 Issue 4

Full text available: pdf(278.45 KB) Additional Information: full citation, abstract, references, index terms

We introduce an approach for power optimization using a set of compilation and architectural techniques. The key technical innovation is a novel divide-and-conquer compilation technique to minimize the number of operations for general computations. Our technique optimizes not only a significantly wider set of computations than the previously published techniques, but also outperforms (or performs at least as well as other techniques) on all examples. Along the architectural dimension, we in ...

Keywords: code generation, transformations

6 Novel techniques in high-level synthesis: Toward efficient static analysis of finite-precision effects in DSP applications via affine arithmetic modeling
Claire Fang Fang, Rob A. Rutenbar, Markus Püschel, Tsuhan Chen
June 2003 **Proceedings of the 40th conference on Design automation**

Full text available: pdf(146.17 KB) Additional Information: full citation, abstract, references, citings, index terms

We introduce a static error analysis technique, based on smart interval methods from *affine arithmetic*, to help designers translate DSP codes from full-precision floating-point to smaller finite-precision formats. The technique gives results for numerical error estimation comparable to detailed simulation, but achieves speedups of three orders of magnitude by avoiding actual bit-level simulation. We show results for experiments mapping common DSP transform algorithms to implementations us ...

Keywords: Static error analysis, affine arithmetic, custom floating-point, embedded hardware, probabilistic error bound

7 A Design of Analog C-Matrix Circuits used for Signal/Data Processing
Takayuki Sugawara, Yoshikazu Miyanaga, Norinobu Yoshida
January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Full text available: pdf(229.30 KB) Additional Information: full citation, abstract

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Various calculation of matrices and vectors has been used in many digital signal processing systems. Although the calculation simply repeats multiplication and addition, the reiteration processing are usually heavy. Therefore, in order to calculate them with high speed, it is necessary to apply parallel proceccing. Although there is another issue that a circuit area becomes large in the case of digital LSI, a proposal analog circuit can realize multiplication and addition simultaneously with the ...

Keywords: Analog Circuit, Signal Processing

8 The state of digital computer technology in Europe
Nelson M. Blachman
June 1961 **Communications of the ACM**, Volume 4 Issue 6

Full text available: pdf(2.16 MB) Additional Information: full citation, abstract, references, citings, index terms

This report indicates the level of computer development and application in each of the thirty countries of Europe, most of which were recently visited by the author

9 TAM Optimization for Mixed-Signal SOCs using Analog Test Wrappers
Anuja Sehgal, Sule Ozev, Krishnendu Chakrabarty
November 2003 **Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(167.79 KB) Additional Information: full citation, abstract, citings, index terms

We present a new approach for TAM optimization and testscheduling in the modular testing of mixed-signal SOCs. A testplanning approach for digital SOCs is extended to handle analogcores in a plug-and-play fashion. A test wrapper based on anADC/DAC pair and a digital configuration circuit is designed foranalog cores such that these cores can be accessed through digitalTAMs. In this way, there is no dependence on an analog testbus and expensive mixed-signal testers. Experimental results arepresent ...

10 Computer-aided digital autopilot design & analysis: Methodology, implementation and verification
W. V. Albanes, J. B. Meadows
December 1979 **Proceedings of the 11th conference on Winter simulation - Volume 1**

Full text available: pdf(663.81 KB) Additional Information: full citation, abstract, references, index terms

This paper details the design methodology for a missile digital autopilot using a digitization approach, and a discrete domain design approach. These two designs rely heavily on computerized system analysis tools in the frequency and time domains. Further, three complex frequency planes are available to the designer, therefore, relative merits of each will be discussed. This paper will also detail the implementation of the autopilot on the missile microcomputer, a six degree of f ...

11 Analog design: A 0.8 µm CMOS switched-capacitor video filter
Antonio Petraglia, Jorge Morales Cañive, Mariane Rembold Petraglia
September 2004 **Proceedings of the 17th symposium on Integrated circuits and system design**

Full text available: pdf(370.63 KB) Additional Information: full citation, abstract, references, index terms

The very low sensitivity properties of switched-capacitor filtering structures implemented as a parallel connection of two allpass sections has already been demonstrated theoretically and verified by computer simulation. This paper describes the design of a fifth-order lowpass elliptic filter using this technique, to satisfy specifications commonly used in video

frequency applications. Operating with a sampling frequency of 16 MHz, the IC prototype was implemented in a standard double-poly CMOS ...

Keywords: allpass circuits, analog integrated circuits, filters, switched-capacitor filters, testing

12 Using codesign techniques to support analog functionality
Francis G. Wolff, Michael J. Knieser, Dan J. Weyer, Chris A. Papachristou
March 1999 **Proceedings of the seventh international workshop on Hardware/software codesign**
Full text available: pdf(433.76 KB) Additional Information: full citation, references, index terms

Keywords: analog, design methodologies, hardware/software codesign

13 Ultra-low-power analog associative memory core using flash-EEPROM-based programmable capacitors
A. Kramer, R. Canegallo, M. Chinosi, D. Doise, G. Gozzini, P. L. Rolandi, M. Sabatini, P. Zabberoni
April 1995 **Proceedings of the 1995 international symposium on Low power design**
Full text available: pdf(136.30 KB) Additional Information: full citation, references, index terms

14 DRAFTS: discretized analog circuit fault simulator
Naveena Nagi, Abhijit Chatterjee, Jacob A. Abraham
July 1993 **Proceedings of the 30th international conference on Design automation**
Full text available: pdf(681.91 KB) Additional Information: full citation, references, citings, index terms

15 Experiences in verifying parallel simulation algorithms
John Penix, Dale Martin, Peter Frey, Ramanan Radhakrishnan, Perry Alexander, Philip A. Wilsey
March 1998 **Proceedings of the second workshop on Formal methods in software practice**
Full text available: pdf(987.99 KB) Additional Information: full citation, references, citings, index terms

16 APL and robotics
A. Martin Euredjian
May 1985 **ACM SIGAPL APL Quote Quad , Proceedings of the international conference on APL: APL and the future**, Volume 15 Issue 4
Full text available: pdf(1.36 MB) Additional Information: full citation, abstract, references, citings, index terms

Program execution speeds on today's general purpose APL running computers do not allow APL to be used as a Robot control language, this execution speed problem will go away with faster and better processors. This paper presents an attempt to make APL work for Robotics with today's technology. The basic concept is quite simple: Leave to APL what it can do in real time and have another computer running a faster language do the rest. This allows for APL program development until the ...

17 ILLIADS: A new fast MOS timing simulator using direct equation-solving approach
Y.-H. Shih, S. M. Kang
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**
Full text available: pdf(675.72 KB) Additional Information: full citation, references, citings, index terms

18 Optical interconnection systems for digital parallel processors
Alexander A. Sawchuk
November 1986 **Proceedings of 1986 ACM Fall joint computer conference**
Full text available: pdf(767.75 KB) Additional Information: full citation, references, index terms

19 Transistor placement for noncomplementary digital VLSI cell synthesis
Michael A. Riepe, Karem A. Sakallah
January 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 1
Full text available: pdf(2.97 MB) Additional Information: full citation, abstract, references, index terms

There is an increasing need in modern VLSI designs for circuits implemented in high-performance logic families such as Cascode Voltage Switch Logic (CVSL), Pass Transistor Logic (PTL), and domino CMOS. Circuits designed in these noncomplementary ratioed logic families can be highly irregular, with complex diffusion sharing and nontrivial routing. Traditional digital cell layout synthesis tools derived from the highly stylized "functional cell" style break down when confronted with such circuit t ...

Keywords: Cell Synthesis, Euler graphs, benchmark circuits, digital circuits, noncomplementary circuits, sequence pair optimization, transistor chaining, transistor placement

20 The development of ODE methods: a symbiosis between hardware and numerical analysis
C. W. Gear, R. Skeel
October 1987 **Proceedings of the ACM conference on History of scientific and numeric computation**
Full text available: pdf(1.11 MB) Additional Information: full citation, abstract, references, index terms

The history of the numerical solution of ordinary differential equations is surveyed from its origins three centuries ago up to the early 1970s. The increasing demands for the solution of ODEs, especially for exterior ballistics and celestial mechanics, has been a primary stimulus of and a significant influence on the early development of computers starting with the analog differential analyzers and continuing to the first wired-program digital computers—whose form foreshadowed future ...